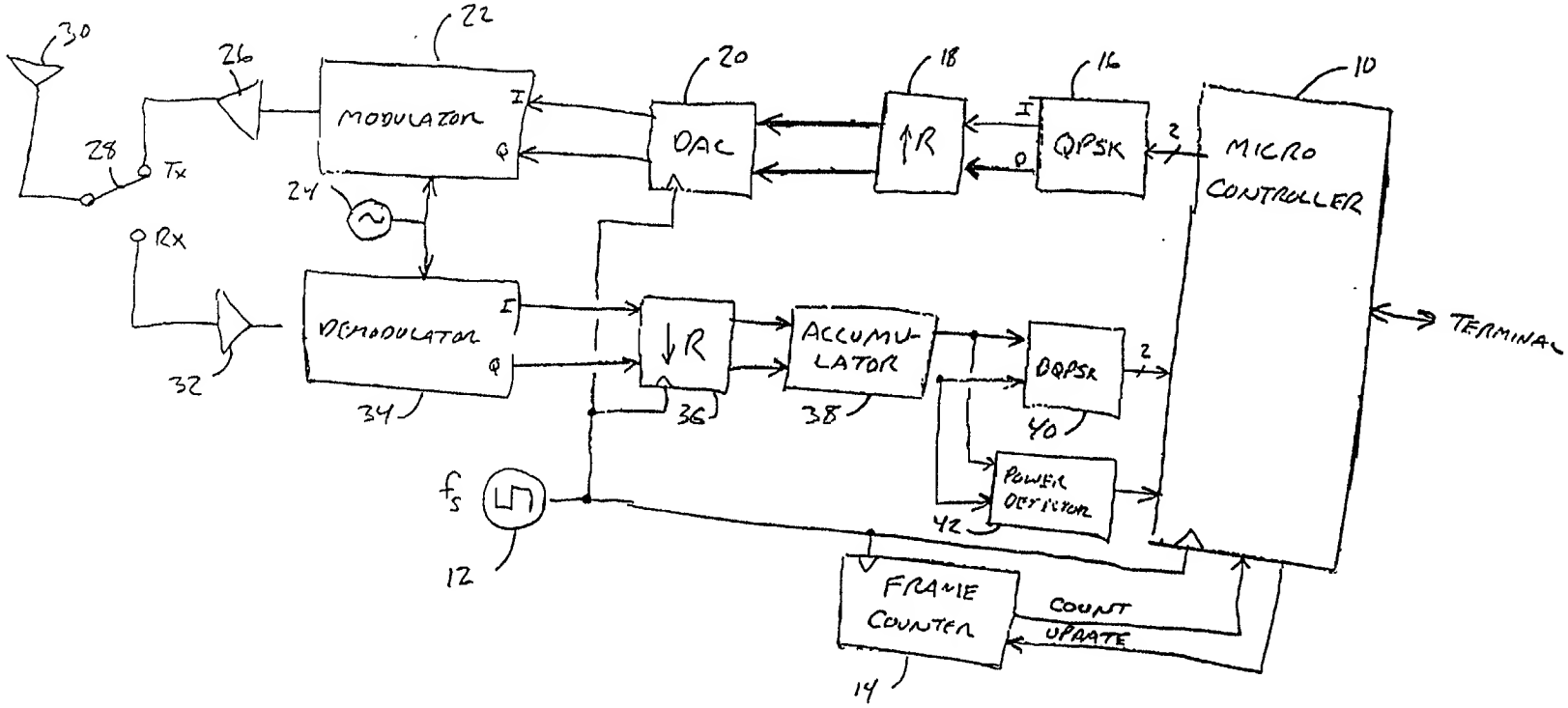
30
26
22
MODULATOR
I
Q
20
DAC
18
↑R
16
I
Q
QPSK
2
10
MICRO CONTROLLER
28
Tx
24
Rx
32
DEMODULATOR
I
Q
34
↓R
36
ACCUMU-LATOR
38
DQPSK
2
40
TERMINAL
f_s
12
POWER DETECTOR
42
FRAME COUNTER
14
COUNT UPDATE

FIGURE 1

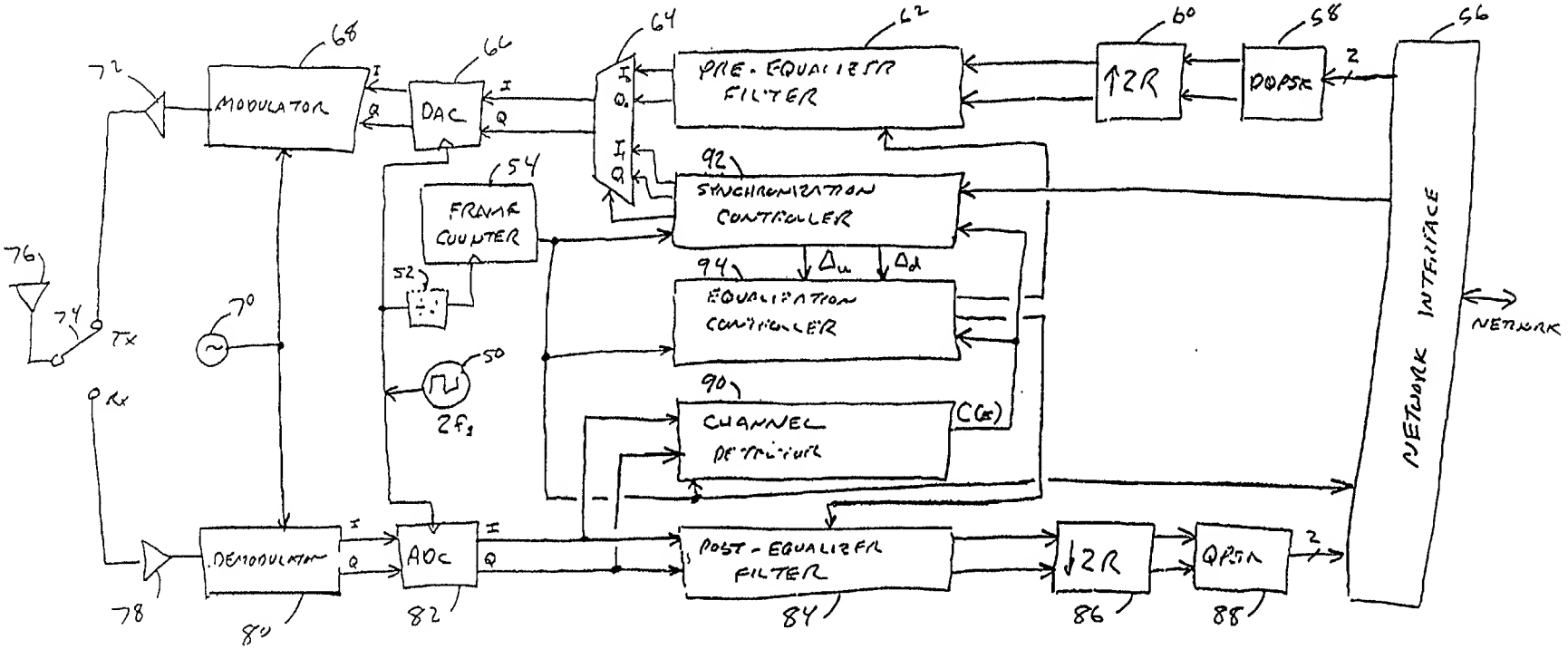
72
MODULATOR
68
DAC
66
I
Q
64
PRE-EQUALIZER FILTER
62
↑2R
60
DQPSK
58
2
56
NETWORK INTERFACE
NETWORK
92
SYNCHRONIZATION CONTROLLER
54
FRAME COUNTER
52
÷
94
EQUALIZATION CONTROLLER
Δ_u
Δ_d
76
74
TX
RX
70
50
$2f_s$
90
CHANNEL DETECTOR
C(z)
DEMODULATION
AOC
POST-EQUALIZER FILTER
↓2R
QPSK
78
80
82
84
86
88

FIGURE 2

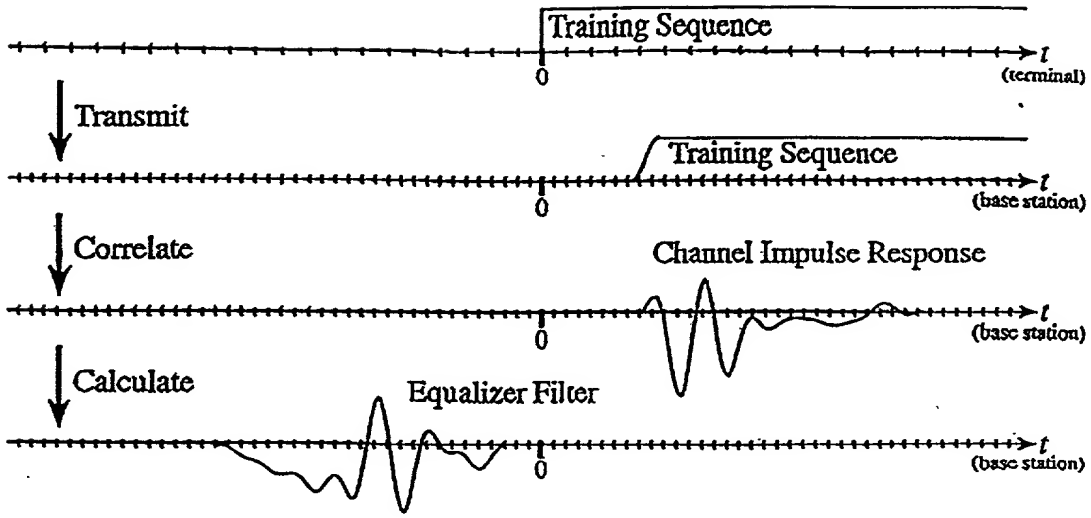

FIGURE 3A

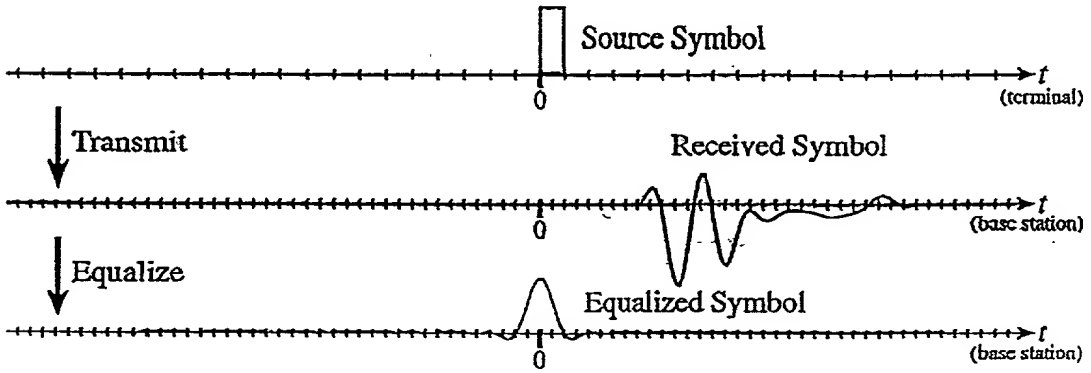

FIGURE 3B

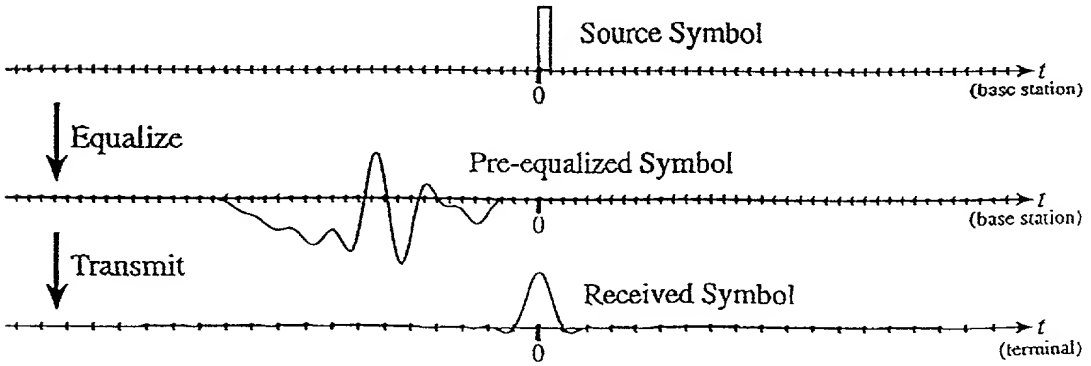

FIGURE 3C

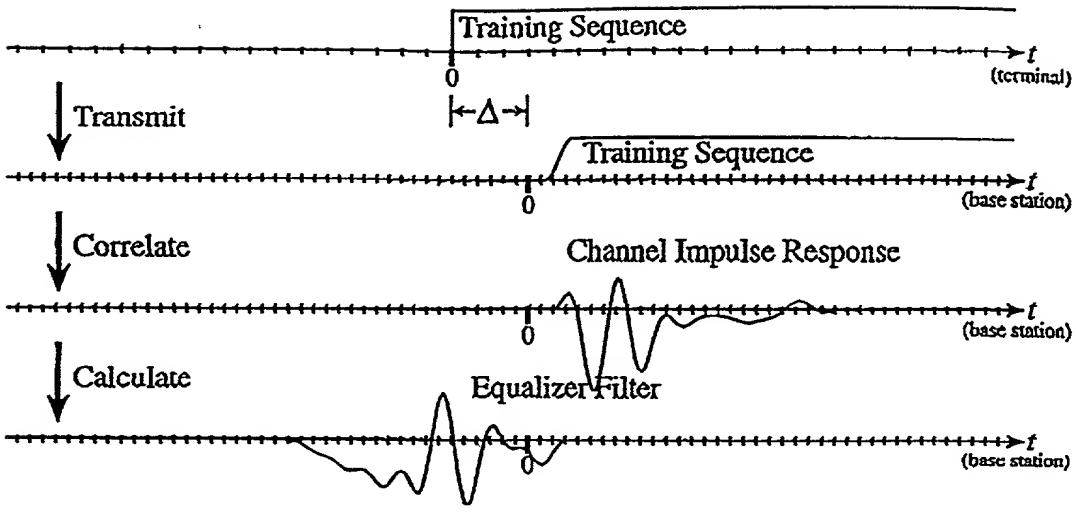

FIGURE 4A

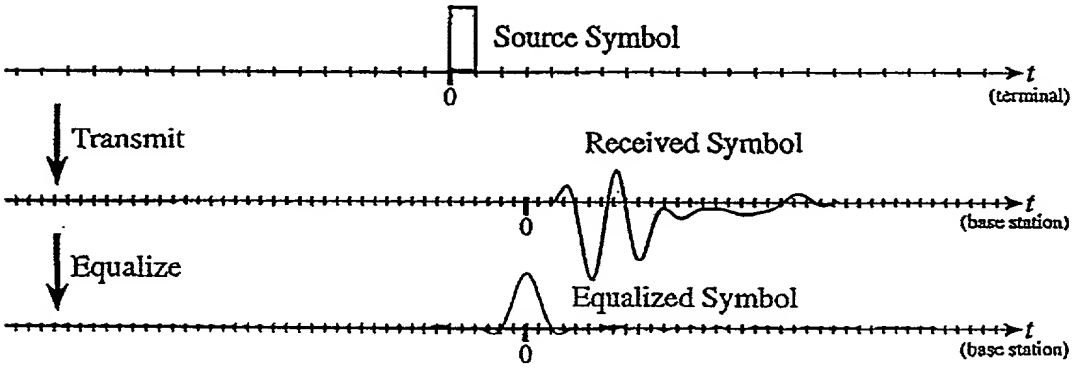

FIGURE 4B

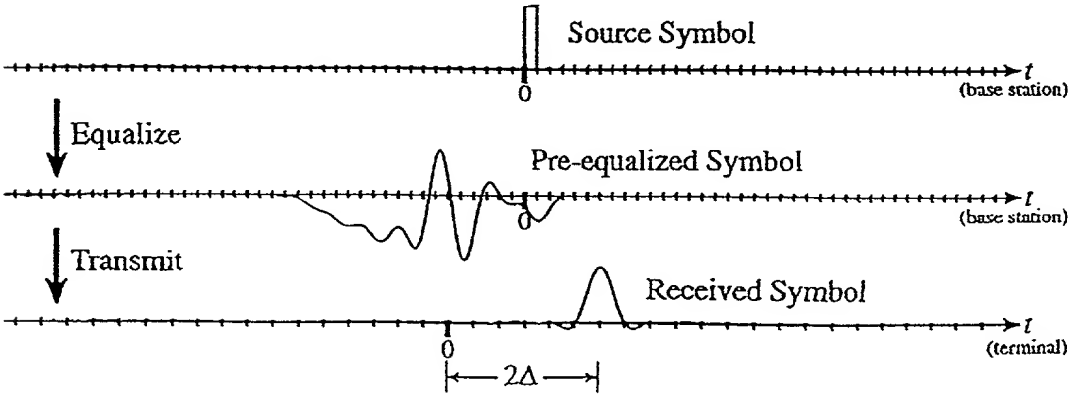

FIGURE 4C

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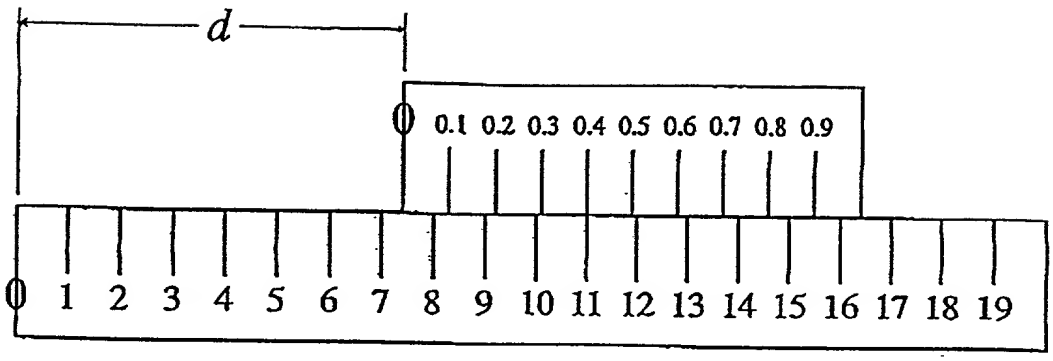

Figure 5

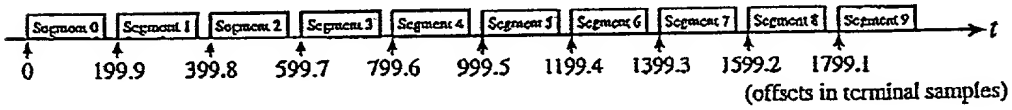

FIGURE 6A

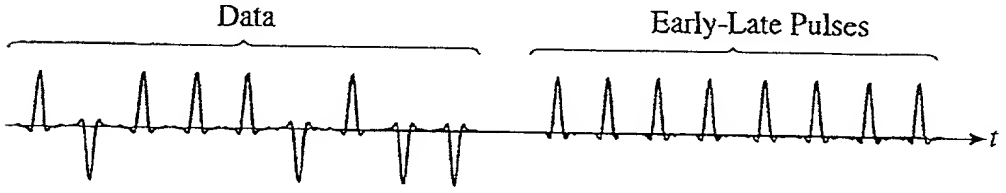

FIGURE 6B

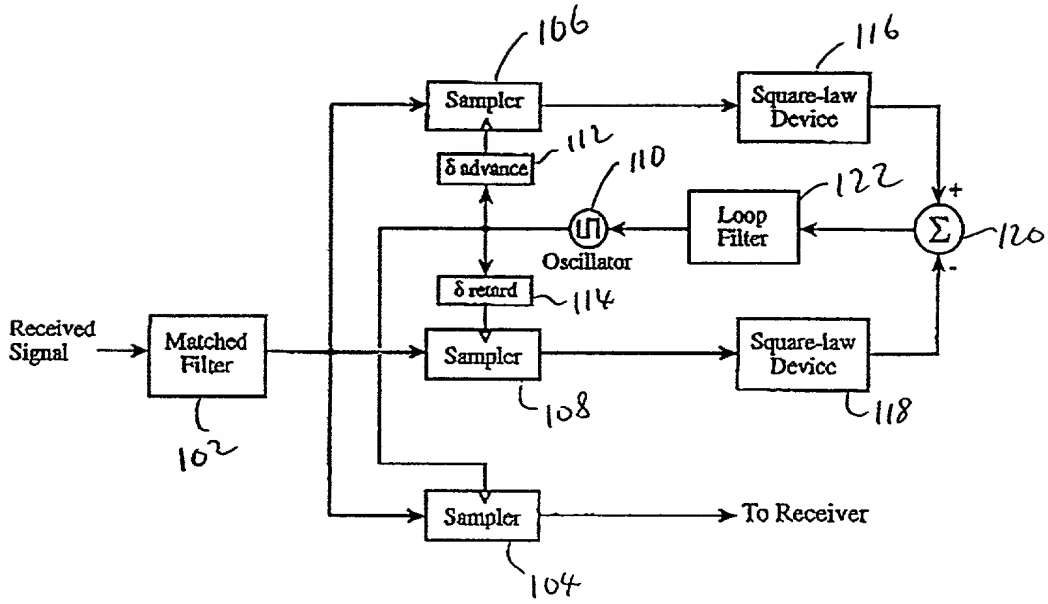
106
116
Sampler
Square-law Device
δ advance
112
110
122
Loop Filter
+
Σ
120
-
Oscillator
δ retard
114
Received Signal
Matched Filter
Sampler
Square-law Device
108
118
102
Sampler
To Receiver
104

Figure 7

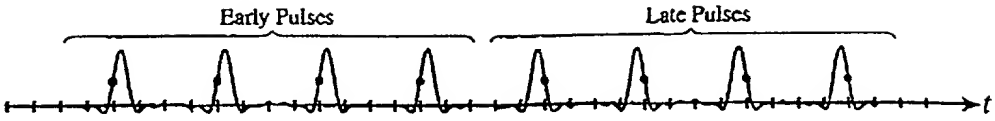

FIGURE 8A

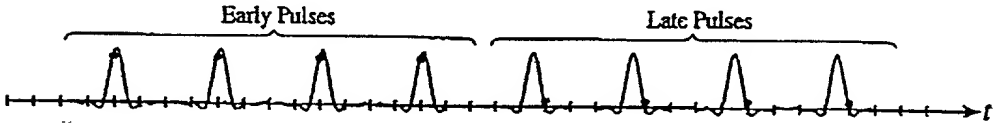

FIGURE 8B

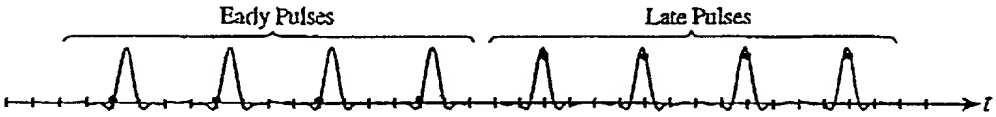

FIGURE 8C

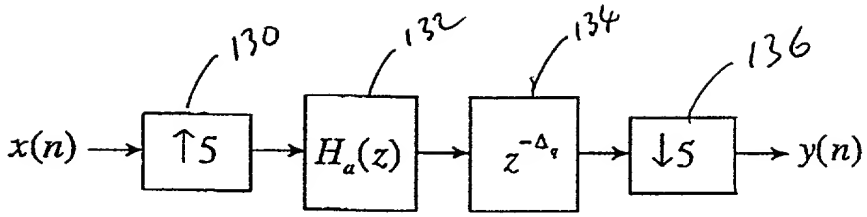

FIGURE 9A

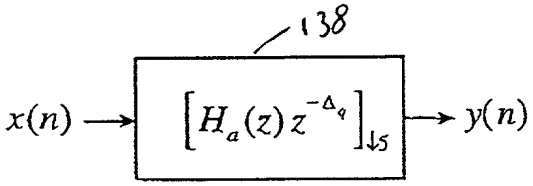

FIGURE 9B

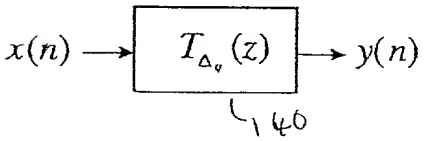

FIGURE 9C

FIGURE 10

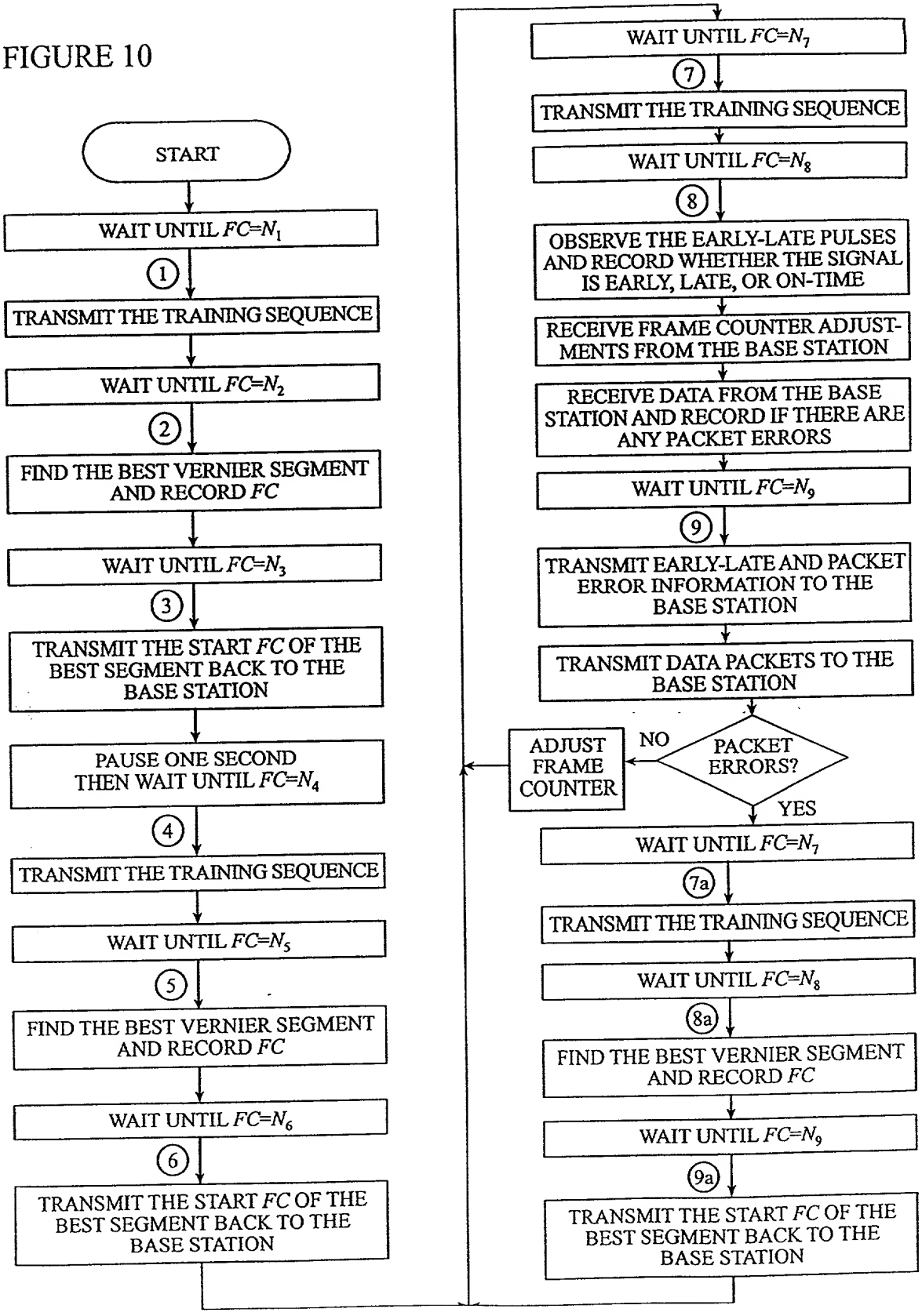

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FIGURE 11

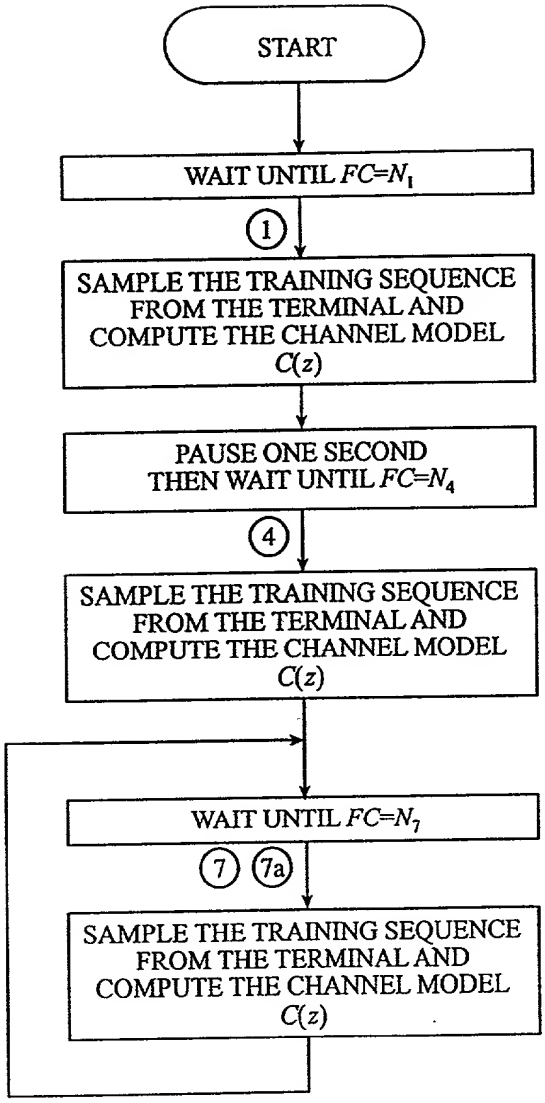

START
WAIT UNTIL $FC=N_1$
1
SAMPLE THE TRAINING SEQUENCE FROM THE TERMINAL AND COMPUTE THE CHANNEL MODEL $C(z)$
PAUSE ONE SECOND THEN WAIT UNTIL $FC=N_4$
4
SAMPLE THE TRAINING SEQUENCE FROM THE TERMINAL AND COMPUTE THE CHANNEL MODEL $C(z)$
WAIT UNTIL $FC=N_7$
7
7a
SAMPLE THE TRAINING SEQUENCE FROM THE TERMINAL AND COMPUTE THE CHANNEL MODEL $C(z)$

FIGURE 12

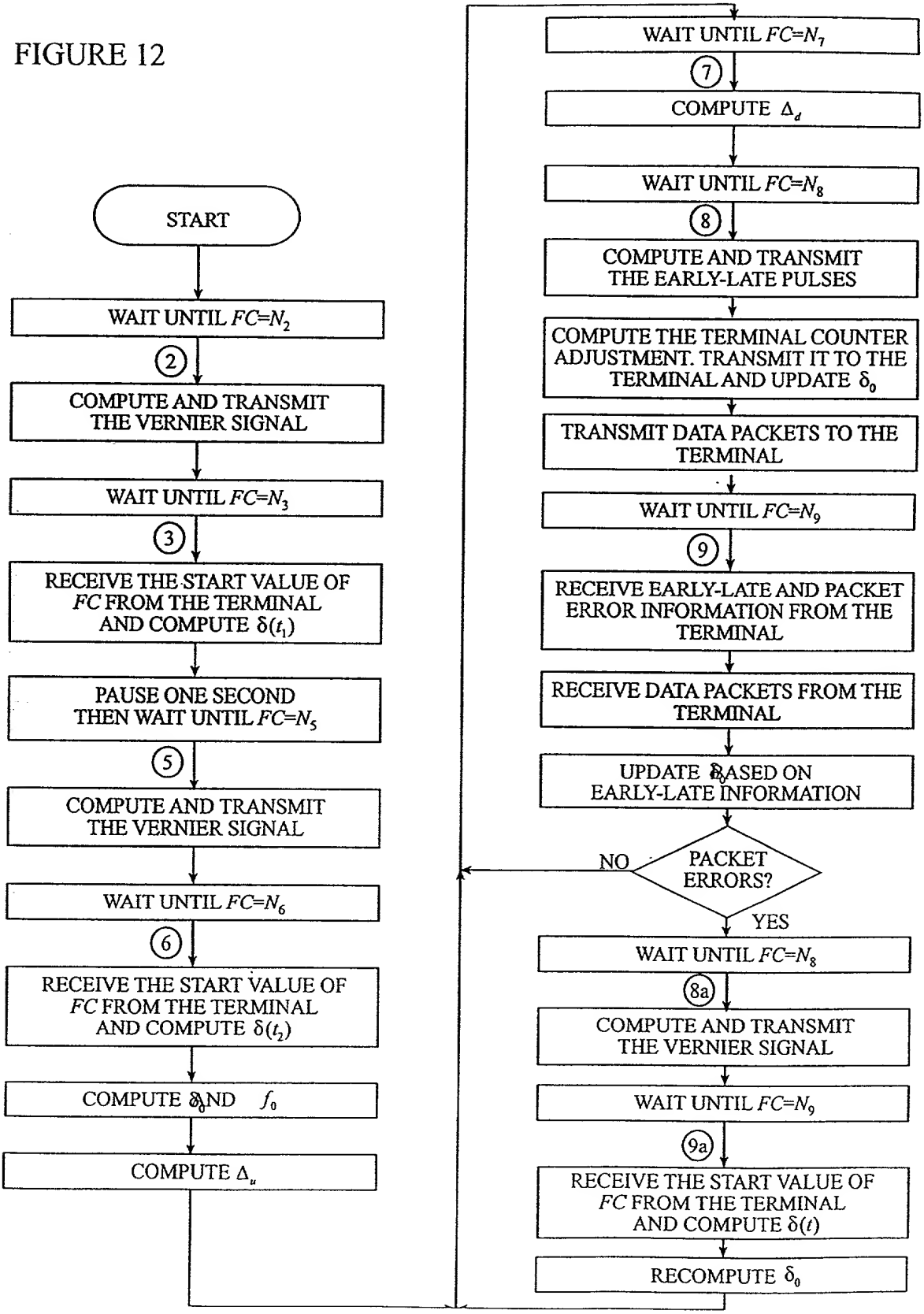
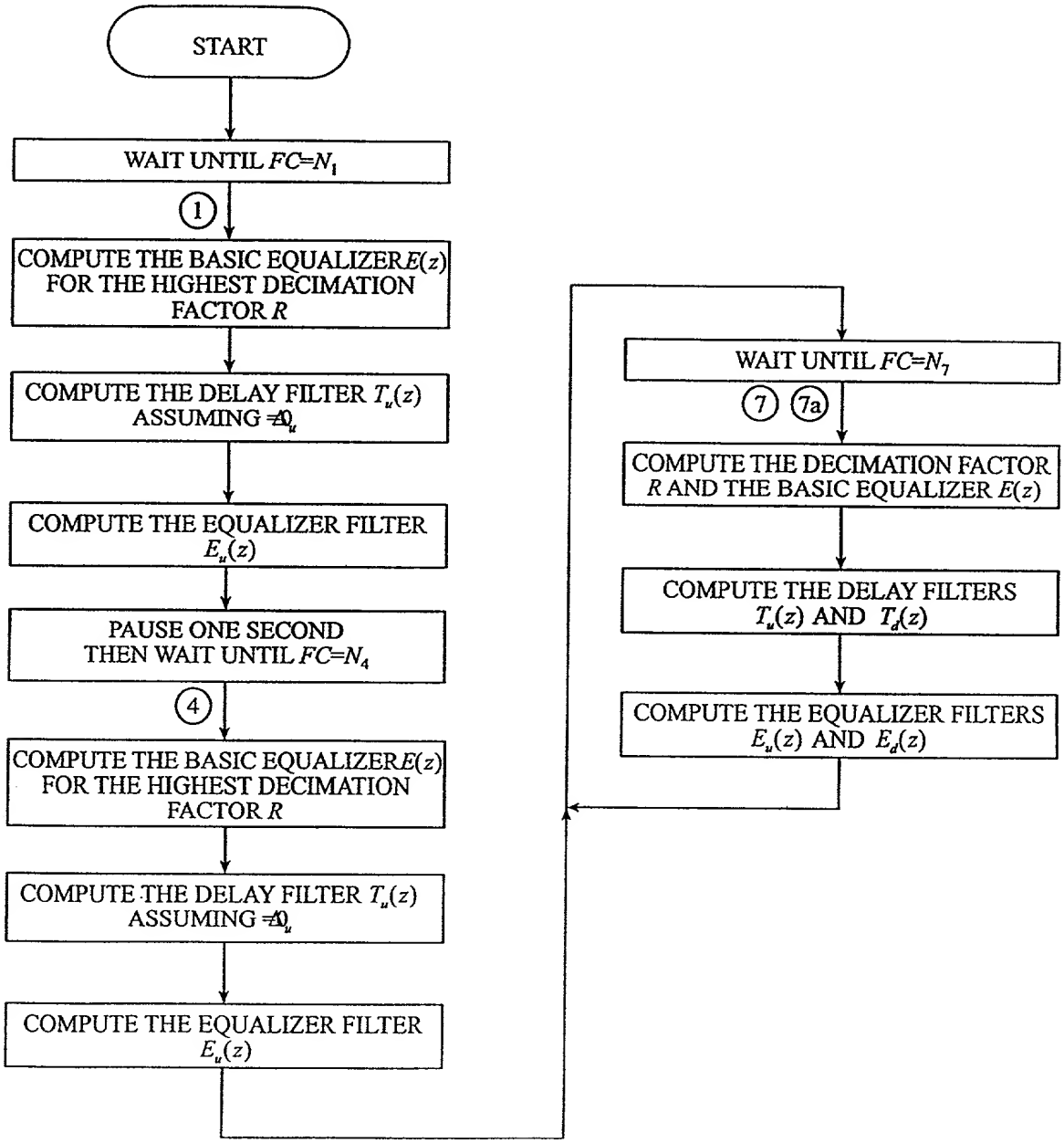

START
WAIT UNTIL $FC=N_2$
2
COMPUTE AND TRANSMIT THE VERNIER SIGNAL
WAIT UNTIL $FC=N_3$
3
RECEIVE THE START VALUE OF FC FROM THE TERMINAL AND COMPUTE $\delta(t_1)$
PAUSE ONE SECOND THEN WAIT UNTIL $FC=N_5$
5
COMPUTE AND TRANSMIT THE VERNIER SIGNAL
WAIT UNTIL $FC=N_6$
6
RECEIVE THE START VALUE OF FC FROM THE TERMINAL AND COMPUTE $\delta(t_2)$
COMPUTE δ_0 AND f_0
COMPUTE Δ_u
WAIT UNTIL $FC=N_7$
7
COMPUTE Δ_d
WAIT UNTIL $FC=N_8$
8
COMPUTE AND TRANSMIT THE EARLY-LATE PULSES
COMPUTE THE TERMINAL COUNTER ADJUSTMENT. TRANSMIT IT TO THE TERMINAL AND UPDATE δ_0
TRANSMIT DATA PACKETS TO THE TERMINAL
WAIT UNTIL $FC=N_9$
9
RECEIVE EARLY-LATE AND PACKET ERROR INFORMATION FROM THE TERMINAL
RECEIVE DATA PACKETS FROM THE TERMINAL
UPDATE δ_0 BASED ON EARLY-LATE INFORMATION
PACKET ERRORS?
NO
YES
WAIT UNTIL $FC=N_8$
8a
COMPUTE AND TRANSMIT THE VERNIER SIGNAL
WAIT UNTIL $FC=N_9$
9a
RECEIVE THE START VALUE OF FC FROM THE TERMINAL AND COMPUTE $\delta(t)$
RECOMPUTE δ_0

FIGURE 13


START
WAIT UNTIL FC=N1
1
COMPUTE THE BASIC EQUALIZER E(z) FOR THE HIGHEST DECIMATION FACTOR R
COMPUTE THE DELAY FILTER Tu(z) ASSUMING =Δu
COMPUTE THE EQUALIZER FILTER Eu(z)
PAUSE ONE SECOND THEN WAIT UNTIL FC=N4
4
COMPUTE THE BASIC EQUALIZER E(z) FOR THE HIGHEST DECIMATION FACTOR R
COMPUTE THE DELAY FILTER Tu(z) ASSUMING =Δu
COMPUTE THE EQUALIZER FILTER Eu(z)
WAIT UNTIL FC=N7
7
7a
COMPUTE THE DECIMATION FACTOR R AND THE BASIC EQUALIZER E(z)
COMPUTE THE DELAY FILTERS Tu(z) AND Td(z)
COMPUTE THE EQUALIZER FILTERS Eu(z) AND Ed(z)